CIO-, PCI-, PCM - QUAD0x board fails to correctly detect the encoder output when signal frequency is larger than a certain value

The QUADx series boards are provided with a built-in digital filter. The purpose of this filter is to eliminate the high frequency noise common in an industrial environment. The Channelx (with x=1...4) Digital Filter Clock Frequency = 10 MHz /(PRESCALERx +1) where PRESCALERx register can take values within the 0-255 range. By default, the PRESCALERx register value is 255. As a result, by default, the Digital Filter Clock Frequency is about 10MHz / 256 = 39.06 kHz and the external encoder output can not be correctly measured over this frequency. This default filter frequency is usually satisfactory for most encoders.

But sometimes, the high-speed encoders' output exceeds 39 kHz. For example, suppose that on channel 1 of a QUAD board we have attached an encoder that provides an output within 0-100 kHz range. In this case, you need to set the Digital Filter Clock Frequency to a value (recommended) ten times larger than 100 kHz (e.g. 1MHz). You need to load the appropriate Prescaler register (PRESCALER1) with a value of 10. In order to do that, you need to use the cbCLoad() or cbCLoad32() Universal Library functions. The cbCLoad() and cbCLoad32() perform the same operation. The only difference between the two is cbCLoad() loads a 16 bit count value and cbCLoad32() loads a 32 bit value. The only time you need to use cbCLoad32() is when loading counts that are larger than 32 bits (counts > 65535).

For more information about programming the QUAD boards series, please refer to the Universal Library Online Manual / Function Reference: cb7266Config(), cbIn32(), cbLoad32(), cbCStatus()

Measurement Computing Data Acquisition Knowledgebase
https://kb.mccdaq.com/KnowledgebaseArticle50108.aspx